

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,276	01/02/2002	Shaun Pendo	047711-0280	6820
75	90 05/17/2005		EXAMINER	
Irvin C. Harrington, III FOLEY & LARDNER			CROSS, LATOYA I	
	ark East, 35th Floor		ART UNIT PAPER NUMBER	
Los Angeles, C			1743	
			DATE MAILED: 05/17/2009	5

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
	10/038,276	PENDO ET AL.	
Office Action Summary	Examiner	Art Unit	
	LaToya I. Cross	1743	
The MAILING DATE of this communication Period for Reply	n appears on the cover sheet w	th the correspondence address	S
A SHORTENED STATUTORY PERIOD FOR RI THE MAILING DATE OF THIS COMMUNICATION - Extensions of time may be available under the provisions of 37 CF after SIX (6) MONTHS from the mailing date of this communication - If the period for reply specified above is less than thirty (30) days, If NO period for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by set any reply received by the Office later than three months after the earned patent term adjustment. See 37 CFR 1.704(b).	ON. FR 1.136(a). In no event, however, may a r in. a reply within the statutory minimum of thir eriod will apply and will expire SIX (6) MON statute, cause the application to become AE	eply be timely filed by (30) days will be considered timely. THS from the mailing date of this commun SANDONED (35 U.S.C. § 133).	nication.
Status			
1) Responsive to communication(s) filed on	01 March 2005.		
·_ ·	This action is non-final.		
3) Since this application is in condition for all	owance except for formal matt	ers, prosecution as to the mer	rits is
closed in accordance with the practice und	der <i>Ex parte Quayl</i> e, 1935 C.D	. 11, 453 O.G. 213.	
Disposition of Claims			
4) ☐ Claim(s) 1.3-14 and 29-38 is/are pending 4a) Of the above claim(s) is/are with 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1.3-14 and 29-38 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction a	ndrawn from consideration.		
Application Papers			
9)☐ The specification is objected to by the Example 1	miner.		
10)☐ The drawing(s) filed on is/are: a)☐	accepted or b) □ objected to	by the Examiner.	
Applicant may not request that any objection to		• • • • • • • • • • • • • • • • • • • •	
Replacement drawing sheet(s) including the co	•	· •	• •
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for for a) All b) Some * c) None of: 1. Certified copies of the priority docum 2. Certified copies of the priority docum 3. Copies of the certified copies of the application from the International But * See the attached detailed Office action for a	nents have been received. nents have been received in A priority documents have been ureau (PCT Rule 17.2(a)).	pplication No received in this National Stag	e
Attachment(s)			
1) Notice of References Cited (PTO-892)	•	Summary (PTO-413)	
2) Notice of Draftsperson's Patent Drawing Review (PTO-948 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SI	·	s)/Mail Date nformal Patent Application (PTO-152)	1
 Information Disclosure Statement(s) (PTO-1449 or PTO/SI Paper No(s)/Mail Date 	6) Other:		

Art Unit: 1743

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 1, 2005 has been entered. Claims 1, 3-14, 29-38 are pending.

Withdrawal of Rejections from Previous Office Action

- The anticipation rejection over Schulman '043 and the obviousness rejections based on Schulman '043 in combination with other references are withdrawn in view of Applicants' amendment to recite the vias as linear hollow paths. Since Schulman '043 teach "stair-stepped" vias, the reference no longer anticipates the claimed invention.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

Art Unit: 1743

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 6, 10-14, 29, 31-34 are rejected under 35 U.S.C. 102(b) as being anticipated by US patent 5,693,577 to Krenik et al.

Krenik et al teach a silicon based biomedical sensor. The sensor comprises a substrate (22) made of silicon ceramic material. On one side of the substrate, there exists an enzyme sensor (42). On the opposite side of the substrate, electrical contacts (30, 32) are disposed. Vias (34, 36) extend from the face of the substrate to the back side of the substrate (figure 3, col. 2, lines 63-65). The vias are formed by depositing impurities into openings (29) and diffusing at 1300°C for 157 hours (hardening step as recited in claims 32-34). The diffusion step creates conductive regions that are hermetically sealed and form a linear hollow path from the sensor side of the substrate to the electronics side of the substrate. At col. 3, lines 18-25, Krenik et al teach that a metal layer (chromium, gold or titanium) is deposited over the front and back side of the substrate and thus over the vias, as recited in claims 10-11. With respect to claim 13, Krenik et al teach multiple vias (34, 36), as shown in figure 3. With respect to claim 31, the reference teaches that the enzyme layer (42) is reactive to human blood, enabling a measurement of the blood sugar level (biological condition) based upon the resistance between the leads (col. 3, lines 48-51). To take resistance measurements, the sensor is

Application/Control Number: 10/038,276 Page 4

Art Unit: 1743

placed in a device (not shown) having contacts in electrical communication with backside contacts (30, 32). Further, with respect to claim 34, figure 4 of Krenik et al show the via being a hollow path disposed from one side of the substrate to the other side of the substrate without interruption.

Claim Rejections - 35 USC § 103

- 4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
- 5. Claims 3, 4, 7, 30, 35-36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krenik et al in view of Wolf et al.

The disclosure of Krenik et al described above. Krenik et al fail to teach 1) alumina substrates and 2) gold as the conductive material to fill the via.

Wolf et al teach implantable medical devices, similar to those disclosed by Schulman et al, having ceramic substrates with sensors and electrodes. The ceramic substrates are taught as alumina or silicon based substrates (col. 6, lines 37-46). Vias (62-68) form conductive paths throughout the substrate. Wolf et al teach the vias may be filled with conductive material such as gold-filled epoxies (col. 9, lines 42-65 and col. 14, line 65 – col. 15, line 3). Further, Wolf et al teach that the vias may be filled by conventional method such as laser cutting, drilling, punching, etc (col. 9, lines 42-50).

Wolf et al also teach that the layered substrate may be laminated together. See (col. 10, lines 1-15 and figure 10, step S106).

Because Wolf et al teach the equivalency of silicon and alumina substrates in biosensors and the conventional use of gold as a conductive material to fill vias in implantable medical devices, it would have been obvious to one of ordinary skill in the art to use alumina substrates and gold material to fill the vias disclosed in Krenik et al to provide a suitable sensor having a conductive passageway through the ceramic substrate.

6. Claims 5 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krenik et al in view of Schulman '808.

The disclosure of Krenik et al is described above. With respect to claims 5 and 37, Krenik et al fail to teach platinum as the conductive material to fill the via.

Schulman '808 teaches an implantable device having a substrate having circuitry and electrically conductive vias. Schulman '808 teaches that the vias are formed of platinum to make the vias hermetic (col. 8, lines 16-29). It would have been obvious to one of ordinary skill in the art to use platinum to fill the vias disclosed in Krenik et al to form a conductive pathway through the structure that also forms a hermetic seal for the pathway.

Art Unit: 1743

7. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krenik et al in view of US patent 5,750,926 to Schulman et al.

Page 6

With respect to claims 8-9, Krenik et al fail to teach a cap covering the electronics side of the device.

Schulman et al teach an implantable sensor device comprising a substrate having electronic circuitry on one side and electrode pairs on the other side. Schulman et al teach that if a cover/lid is provided(40), the electronic circuitry is shrouded and provided with a protective housing. See col. 7, lines 3-14. It would have been obvious to one of ordinary skill in the art to incorporate a cover (lid) over the electronics side of the device in Krenik et al to allow the device to operate in environments that would ordinarily be harmful to the electronic circuitry.

Response to Arguments

8. Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Pertinent Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US patent 5,569,958 to Bloom teaches a chip package comprised of a substrate (20) having circuit traces (24, 25) on both sides of the substrate and conductive vias (30) that are hermetically sealed and are disposed from one side of the substrate to the other side of the substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaToya I. Cross whose telephone number is 571-272-1256. The examiner can normally be reached on Monday-Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jill A. Warden can be reached on 571-272-1267. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 1743

Page 8

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

lic

Supervisory Patent Examiner
Technology Center 1700